

LIPERS
力垣企業股份有限公司
LIPERS ENTERPRISE CO., LTD.



DATA SHEET

Multi-Layer Ceramic Chip Capacitor

Standard Type Series of MLCC





Contents

- 1. Product Identification**
- 2. Standard Combination of Nominal Capacitance and Tolerance**
- 3. Dimension & Structure**
- 4. Capacitance Value Range**
- 5. Reliability and Test Conditions**
- 6. P.C. Board for Bending Strength Test**
- 7. Test Substrate**
- 8. Packaging**
- 9. Precaution of Usage**
- 10. Caution: Handling After Chip Mounted**



UWA Multi-Layer Ceramic Chip Capacitor

***** Standard Type of MLCC *****

Features

- Nickel barrier end terminations to improve solder ability.
- Multilayer block structure provides higher reliability.
- A wide range of capacitance values available in standard case sizes.

Applications

- General Electronic Devices.

1. Product Identification

M	0603	N	101	J	050	T	A	X
1-1	1-2	1-3	1-4	1-5	1-6	1-7	1-8	1-9

1-1. **M** UWA Standard Type MLCC (M Series)

1-2. **0603** Size

Code	EIA Code	Length * Width mm / (inch)
01005	01005	$(0.40\pm 0.02) * (0.20\pm 0.02) / (0.016\pm 0.0008) * (0.008\pm 0.0008)$
0201	0201	$(0.60\pm 0.03) * (0.30\pm 0.03) / (0.024\pm 0.001) * (0.012\pm 0.001)$
0402	0402	$(1.00\pm 0.05) * (0.50\pm 0.05) / (0.04\pm 0.002) * (0.02\pm 0.002)$
0603	0603	$(1.60\pm 0.10) * (0.80\pm 0.10) / (0.06\pm 0.006) * (0.03\pm 0.006)$
0805	0805	$(2.00\pm 0.20) * (1.25\pm 0.20) / (0.08\pm 0.008) * (0.05\pm 0.008)$
1206	1206	$(3.20\pm 0.30) * (1.60\pm 0.20) / (0.12\pm 0.008) * (0.06\pm 0.008)$
1210	1210	$(3.20\pm 0.30) * (2.50\pm 0.20) / (0.12\pm 0.008) * (0.10\pm 0.008)$
1812	1812	$(4.50\pm 0.40) * (3.20\pm 0.30) / (0.18\pm 0.012) * (0.12\pm 0.012)$
2220	2220	$(5.70\pm 0.40) * (5.00\pm 0.40) / (0.22\pm 0.016) * (0.20\pm 0.016)$

1-3. **N** Temperature Characteristic

Code	Temperature Characteristic	Capacitance Change	Operation Temperature Range
N	NPO	±30 PPM	-55°C ~ +125°C
X	X7R	±15 %	-55°C ~ +125°C
Y	Y5V	+22 ~ -82 %	-30°C ~ +85°C
B	X5R	±15 %	-55°C ~ +85°C
S	X6S	±22 %	-55°C ~ +105°C
R	X5S	±22 %	-55°C ~ +85°C
E	Y5U	+22 ~ -56 %	-30°C ~ +85°C
Z	Z5U	+22 ~ -56 %	+10°C ~ +85°C

1-4. **101** Capacitance Value

Code	Capacitance (pF)	Code	Capacitance (pF)
0R5	0.5	101	100
010	1	104	100,000 (100nF)
100	10	106	10,000,000 (10uF)



UWA Multi-Layer Ceramic Chip Capacitor

1-5. J Capacitance Tolerance

Code	Tolerance	Nominal Capacitance
B	± 0.1 pF	≤ 10 pF
C	± 0.25 pF	
D	± 0.5 pF	
F	± 1 %	≥ 10 pF
G	± 2 %	
H	± 3 %	
J	± 5 %	
K	± 10 %	
M	± 20 %	
Z	- 20 ~ + 80 %	

1-6. 050 Rated Voltage

Code	Rated Voltage	Code	Rated Voltage
006	6.3V	025	25V
010	10V	050	50V
016	16V		

1-7. T Quantity

(Unit : pcs)

Code	A	B	T	U	V	W	X	Y	Z	E		
7 //	15K	10K	4K	3K	2.5K	2K	1K	700	500	20K		
Code	F	G	H	I	J	Code	L	M	N	R	P	Q
13 //	50K	15K	10K	4K	2K	Bulk	5K	10K	20K	50K	100K	200K

1-8. A Chip Thickness

(Unit : mm)

Code	P	K	V	T	A	D	S	E	Q
Thickness	0.3±0.03	0.45±0.05	0.5±0.05	0.7±0.1	0.8±0.1	0.85±0.1	0.65±0.1	1.0±0.1	0.2±0.02
Code	F	G	H	L	N	Y	M	U	
Thickness	1.15±0.1	1.25±0.2	1.5±0.2	1.6±0.2	1.9±0.2	2.0±0.2	2.5±0.2	3.2±0.3	

1-9. N Material Option

Code	Description Of The Code
N	Sn – Pb Plating (Sn 90% , Pb 10%)
X	Pb – Free Plating (Sn 100%)

SPECIAL TOLERANCE

N=Nomal Size

(Unit : mm)

Size Code	01005	0201	0402	0603	0805	1206	1210	1812
1	N±0.03	N±0.05	N±0.07	N±0.07	N±0.15	N±0.15	N±0.20	N±0.20
2	N±0.05	N±0.07	N±0.10	N±0.15	N±0.20	N±0.20	N±0.30	N±0.40
3	N±0.07	N±0.09	N±0.15	N±0.20	N±0.30	N±0.30		
4	N±0.09		N±0.20	N±0.25				
5			N±0.40	N±0.30				
6			N±0.30					

NOTE: Product range might be extended due to technology improvement or new product released, please contact our sales.



UWA Multi-Layer Ceramic Chip Capacitor

2. Standard Combination of Nominal Capacitance and Tolerance

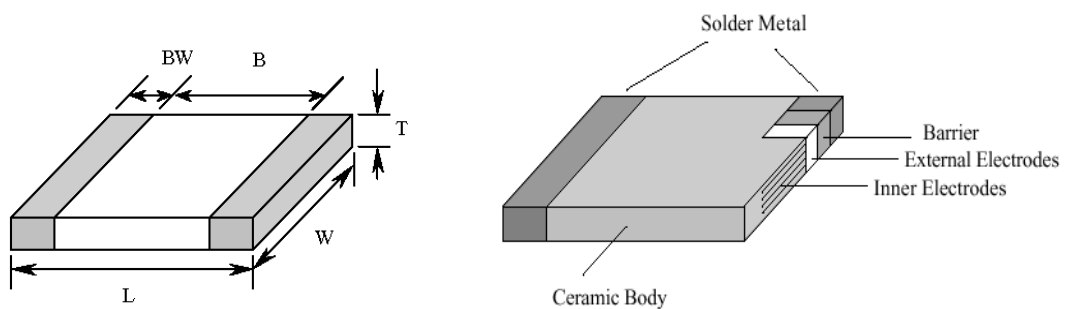
Class	Temperature Characteristic	Tolerance		Nominal Capacitance
Class I	NPO	Less Than 10pF	B(± 0.10 pF)	0.5,1,1.5,2,2.5,3
			C(± 0.25 pF)	0.5,1,1.5,2,2.5,3,3.5,4,4.5,5
			D(± 0.50 pF)	5,6,7,8,9,10
			F(± 1.00 pF)	6,7,8,9,10
		More Than 10pF	J($\pm 5\%$)	E-24 series
B($\pm 10\%$)				
Class II	X7R / X5R X5S / X6S	K($\pm 10\%$) , M($\pm 20\%$)		E-12 series
	Y5V	M($\pm 20\%$) , Z(-20 ~ +80%)		E- 6 series
	Y5U			
	Z5U			

	Application Capacitance											
E-3	1.0				2.2				4.7			
E-6	1.0		1.5		2.2		3.3		4.7		6.8	
E-12	1.0	1.2	1.5	1.8	2.2	2.7	3.3	3.9	4.7	5.6	6.8	8.2
E-24	1.0	1.2	1.5	1.8	2.2	2.7	3.3	3.9	4.7	5.6	6.8	8.2
	1.1	1.3	1.6	2.0	2.4	3.0	3.6	4.3	5.1	6.2	7.5	9.1

3. Dimension & Structure

(Unit : mm)

Code	L	W	T(max)	BW(min)
01005	0.40 \pm 0.02	0.20 \pm 0.02	0.22	0.07
0201	0.60 \pm 0.03	0.30 \pm 0.03	0.33	0.15
0402	1.00 \pm 0.05	0.50 \pm 0.05	0.55	0.20
0603	1.60 \pm 0.10	0.80 \pm 0.10	0.95	0.20
0805	2.00 \pm 0.20	1.25 \pm 0.20	1.40	0.20
1206	3.20 \pm 0.30	1.60 \pm 0.20	1.80	0.30
1210	3.20 \pm 0.30	2.50 \pm 0.20	2.70	0.30
1812	4.50 \pm 0.40	3.20 \pm 0.30	3.30	0.30
2220	5.70 \pm 0.40	5.00 \pm 0.40	3.00	0.30





UWA Multi-Layer Ceramic Chip Capacitor

4. Capacitance Value Range

Size Code		Capacitance Range				
		Class I	Class II			
		NPO	X7R	X6S	X5R	Y5V
01005	4V				15nF~47nF	
	6.3V	100pF			680pF~220nF	
	10V		100pF~1nF		470pF~10nF	
	16V	0.5pF~22pF				
	25V	0.5pF~27pF		100nF		
0201	4V			2.2nF~10nF	100nF~2.2uF	
	6.3V	100pF	2.2nF~10nF	100nF	330pF~2.2uF	22nF~470nF
	10V		470pF~10nF		2.2nF~2.2uF	
	16V		100pF~10nF		220pF~1uF	
	25V	0.20pF~100pF	220pF~10nF		1nF~100nF	
	50V	0.20pF~100pF	220pF~1nF			
0402	2.5V			2.2uF		
	4V			100nF~10uF	100nF~22uF	
	6.3V		47nF~470nF			10nF~4.7uF
	10V	560pF~910pF	100pF~470nF	100nF~1uF	15nF~10uF	10nF~1uF
	16V	33pF~1.2nF	100pF~220nF		15nF~4.7uF	10nF~330nF
	25V	0.5pF~1.8nF	100pF~100nF	1uF	100nF~2.2uF	10nF~100nF
	35V				100nF~1uF	
	50V	0.5pF~1.8nF	100pF~47nF			10nF~100nF
0603	4V			100nF~22uF	100nF~47uF	
	6.3V		47nF~10uF			10nF~4.7uF
	10V		100pF~2.2uF	100nF~10uF	100nF~22uF	
	16V	68pF~3.9nF	100pF~1uF			10nF~2.2uF
	25V	0.5pF~10nF		100nF~4.7uF	100nF~10uF	1nF~2.2uF
	50V	0.5pF~6.8nF	100pF~330nF		100nF~2.2uF	10nF~1uF
0805	2.5V			22uF~47uF		
	4V			100nF~47uF	100nF~47uF	
	6.3V		47nF~10uF	100nF~22uF		6.8uF~22uF
	10V					2.2uF~22uF
	16V			100nF~10uF	100nF~22uF	100nF~10uF
	25V	220pF~33nF	47nF~4.7uF			100nF~4.7uF
	50V	0.50pF~27nF	47nF~1uF		100nF~4.7uF	10nF~1uF
1206	4V			10uF~47uF		
	6.3V		47nF~47uF	100nF~100uF	100nF~100uF	10uF
	10V			100nF~47uF		6.8uF~22uF
	16V	120nF	47nF~22uF	100nF~22uF	100nF~22uF	1uF~22uF
	25V	330pF~100nF				100nF~10uF
	50V	0.5pF~68nF			100nF~10uF	100nF~1uF
	1210	4V			100uF	
6.3V			47nF~47uF	100nF~100uF	22uF~100uF	
10V						
16V			47nF~22uF	100nF~47uF	4.7uF~100uF	22uF/47uF
25V		10nF			4.7uF~47uF	4.7uF~22uF
35V				100nF~22uF	2.2uF~22uF	10uF/22uF
50V		560pF~47nF	47nF~10uF		4.7uF~10uF	
				2.2uF~10uF	10uF	

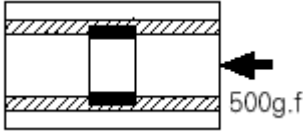
Note : (1) Other size, capacitance, and voltage are available upon customer's request.

(2) Product range might be extended due to technology improvement or new product released, please contact our sales.



UWA Multi-Layer Ceramic Chip Capacitor

5. Reliability and Test Conditions

No	Test Item	Specifications	Test Conditions			
1	Capacitance Class I NPO	Within The Specified Tolerance	Capacitance	Frequency	Signal Voltage	
			$C \leq 1000 \text{ pF}$	$1\text{MHz} \pm 10\%$	$1.0 \pm 0.2\text{Vrms}$	
			$C > 1000 \text{ pF}$	$1\text{KHz} \pm 10\%$	$1.0 \pm 0.2\text{Vrms}$	
	Capacitance Class II	Within The Specified Tolerance	Capacitance	Temp.Char.	Frequency	Rated Voltage
$C \leq 10\mu\text{F}$			X7R / X5R	$1\text{KHz} \pm 10\%$	$1.0 \pm 0.2\text{Vrms}$	
			X6S / X5S	$1\text{KHz} \pm 10\%$	$1.0 \pm 0.2\text{Vrms}$	
			Y5V	$1\text{KHz} \pm 10\%$	$1.0 \pm 0.2\text{Vrms}$	
$C > 10\mu\text{F}$	$120\text{Hz} \pm 20\%$	$0.5 \pm 0.1\text{Vrms}$				
2	Q Class I NPO	$C > 30 \text{ pF} : Q \geq 1000$ $C \leq 30 \text{ pF} : Q \geq 400 + 20 \times C$ (C:Capacitance , pF)	Capacitance	Frequency	Signal Voltage	
			$C \leq 1000 \text{ pF}$	$1\text{MHz} \pm 10\%$	$1.0 \pm 0.2\text{Vrms}$	
			$C > 1000 \text{ pF}$	$1\text{KHz} \pm 10\%$	$1.0 \pm 0.2\text{Vrms}$	
	Tan δ (D.F.) Class II	Shall meet the value in Table 1	Capacitance	Temp.Char.	Frequency	Signal Voltage
$C \leq 10\mu\text{F}$			X7R / X5R	$1\text{KHz} \pm 10\%$	$1.0 \pm 0.2\text{Vrms}$	
			X6S / X5S	$1\text{KHz} \pm 10\%$	$1.0 \pm 0.2\text{Vrms}$	
Y5V	$1\text{KHz} \pm 10\%$	$1.0 \pm 0.2\text{Vrms}$				
ALL	$C > 1\mu\text{F}$	$120\text{Hz} \pm 10\%$	$0.5 \pm 0.1\text{Vrms}$			
3	(I.R.) Insulation Resistance	Rated Voltage $\geq 25\text{V}$ $10,000 \text{ M}\Omega$ or $500\text{M}\Omega \div \mu\text{F}$ Rated Voltage $\leq 16\text{V}$ $10,000 \text{ M}\Omega$ or $100 \text{ M}\Omega \div \mu\text{F}$ Product Whichever Is Smaller	$V_r \leq 500\text{V}$ Applied Voltage: Rated Voltage $V_r \geq 500\text{V}$ Applied Voltage: 500V Applied Voltage: Rated Voltage Charge Time : 60 sec.			
4	Withstanding Voltage	No Dielectric Breakdown or Mechanical Breakdown	$V_r < 100\text{V}$ Class I:300% of The Rated Voltage Class II:250% of The Rated Voltage $V_r = 100\text{V}$ 250% of The Rated Voltage $250\text{V} \leq V_r < 500\text{V}$ 200% of The Rated Voltage $500\text{V} \leq V_r < 1\text{KV}$ 150% of The Rated Voltage $V_r \geq 1\text{KV}$ 120% of The Rated Voltage For 1~5 sec. Is Applied Less Than 50mA Current			
5	Adhesive Strength Of Termination	No Indication Of Peeling Shall Occur On The Terminal Electrode.	A 500g..f Push or Pull Force Shall Be Applied For 10 ± 1 Seconds 			
6	Resistance To Flexure Of Substrate	No Mechanical Damage Shall Occur.		Bending Shall Be Applied To The 1.0 mm		
		C-Meter	Temp. Char.	Cap. Change.	With 1.0 mm/sec	
			NPO	$\leq \pm 5 \%$		
			X7R / X5R X6S / X5S	$\leq \pm 12.5 \%$		
			Y5V	$\leq \pm 30 \%$		
Y5U						
Z5U						



UWA Multi-Layer Ceramic Chip Capacitor

		Chip Array Capacitor				
		NPO	$\leq \pm 1 \%$			
		X7R	$\leq \pm 10 \%$			
Y5V						
7	Vibration	No Mechanical Damage Shall Be Occur			Vibrate The Capacitor With Amplitude Of 1.5mm P-P Changing The Frequencies From 10Hz to 55Hz And Back To 10Hz In About 1 min.	
		Capacitance	Temp. Char.			Cap. Change
			Class I	NPO		Within $\pm 2.5\%$ Or $\pm 0.25\text{pF}$ Whichever Is Larger
			Class II	X7R / X5R X6S / X5S Y5V/Y5U/Z5U		Within $\pm 7.5 \%$ Within $\pm 20 \%$
		Q Class I	C > 30 pF : Q ≥ 1000 C ≤ 30 pF : Q $\geq 400 + 20 \times C$			
		Tan δ Class II	To Satisfy The Specified Initial Value			
		Insulation Resistance	To Satisfy The Specified Initial Value			
8	Capacitance Temperature Coefficient	Class I	Temp.Char.	Temp. Range	Cap. Change	Class I :
			NPO	$-55^{\circ}\text{C} \sim +125^{\circ}\text{C}$	$\pm 30 \text{ ppm} / ^{\circ}\text{C}$	
		Class II	Temp.Char.	Temp. Range	Cap. Change	Class II :
			X7R	$-55^{\circ}\text{C} \sim +125^{\circ}\text{C}$	$\pm 15 \%$	
			X5R	$-55^{\circ}\text{C} \sim +85^{\circ}\text{C}$	$\pm 15 \%$	
			X5S	$-55^{\circ}\text{C} \sim +85^{\circ}\text{C}$	$\pm 22 \%$	
			X6S	$-55^{\circ}\text{C} \sim +105^{\circ}\text{C}$	$\pm 22 \%$	
			Y5V	$-30^{\circ}\text{C} \sim +85^{\circ}\text{C}$	$+ 22 \% \sim - 82 \%$	
			Y5U	$-30^{\circ}\text{C} \sim +85^{\circ}\text{C}$	$+ 22 \% \sim - 56 \%$	
Z5U	$+10^{\circ}\text{C} \sim +85^{\circ}\text{C}$	$+ 22 \% \sim - 56 \%$				
					$\frac{C2-C1}{C1(T2-T1)} \times 100\%$ $\frac{C2-C1}{C1} \times 100\%$	
					T1: Standard Temperature (25°C) T2: Test Temperature C1: Capacitance At Standard Temperature (25°C) C2: Capacitance At Test Temperature (T2)	



UWA Multi-Layer Ceramic Chip Capacitor

12	High Temperature	No Mechanical Damage Shall Be Occur						<p>Class II capacitors applied DC voltage is applied for one hour at maximum operation temperature $\pm 3^{\circ}\text{C}$ then shall be set for 48 ± 4 hours at room temperature and the initial measurement shall be conducted.</p> <p>Applied Voltage : $V_r \leq 200\text{V}$: 200% Of Rated Voltage $V_r \geq 250\text{V}$: 120% Of Rated Voltage Temperature : Maximum Operation Temperature Test Time : 1000 +48/-0 Hour Current Applied: 50mA Max. Measurement Room Temperature After Cooling For : Class I : 24 ± 2 Hour Class II : 48 ± 4 Hour</p>	
		Capacitance	Temp. Char.			Cap. Change			
			Class I	NPO		Within $\pm 3.0\%$ Or $\pm 0.3\text{pF}$ Whichever Is Larger			
		Class II	X7R / X5R X6S / X5S		Within $\pm 15\%$				
			Y5V/Y5U/Z5U		Within $\pm 30 \sim 40\%$				
Q Class I	$C > 30\text{pF}$: $Q \geq 350$ $10\text{pF} < C \leq 30\text{pF}$: $Q \geq 275 + 2.5 \times C$ $C \leq 10\text{pF}$: $Q \geq 200 + 10 \times C$								
Tan δ Class II	Temp. Char.	HI-V	50V	25V	16V	10V	6.3V		
	X7R / X5R X6S / X5S	5%	5%	7%	7%	10%	12.5%		
	Y5V	7.5%	7.5%	10.5%	12.5%	15%	20%		
	Y5U / Z5U	5%	6%	10.5%	10.5%	-	-		
13	Humidity	No Mechanical Damage Shall Be Occur						<p>Class II capacitor shall be set for 48 ± 4 hours at room temperature after one hour heat treatment at $150 \pm 0/-10^{\circ}\text{C}$ before initial measure.</p> <p>Applied Voltage : Rated Voltage Temperature : $40 \pm 2^{\circ}\text{C}$ Relative Humidity : 90 ~ 95 % RH Test Time : 500+12/-0 Hour Current Applied: 50mA Max. Measurement Room Temperature After Cooling For: Class I : 24 ± 2 Hours Class II : 48 ± 4 Hours</p>	
		Capacitance	Temp. Char.			Cap. Change			
			Class I	(NPO)		Within $\pm 5\%$ Or $\pm 0.5\text{pF}$ Whichever Is Larger			
			Class II	X7R / X5R		Within $\pm 15\%$			
		Y5V/Y5U/Z5U		Within $\pm 30\%$					
		Q Class I	$C > 30\text{pF}$: $Q \geq 350$ $10\text{pF} < C \leq 30\text{pF}$: $Q \geq 275 + 2.5 \times C$ $C \leq 10\text{pF}$: $Q \geq 200 + 10 \times C$						
		Tan δ Class II	Temp. Char.	HI-V	50V	25V	16V		10V
X7R / X5R X6S / X5S	2.5%		5%	7%	7%	10%	12.5%		
Y5V	7.5%		7.5%	10.5%	12.5%	15%	20%		
Y5U / Z5U	5%		6%	6%	6%	-	-		
Insulation Resistance	Minimum Insulation Resistance : 1000 M Ω or 50 M Ω \times uF product whichever is smaller								
14	Humidity Load	No Mechanical Damage Shall Be Occur						<p>Class II capacitors applied DC voltage of the rated voltage is applied for one hour at maximum operation temperature $\pm 3^{\circ}\text{C}$ then shall be set for 48 ± 4 hours at room temperature and the initial measurement shall be conducted</p>	
		Capacitance	Temp. Char.			Cap. Change			



UWA Multi-Layer Ceramic Chip Capacitor

		Class I	NPO	Within $\pm 7.5\%$ Or $\pm 0.75\text{pF}$ Whichever Is Larger				Applied Voltage : Rated Voltage Temperature : $40 \pm 2^\circ\text{C}$ Relative Humidity : 90 ~ 95% RH Test Time : 500 + 12 / - 0 Hour Current Applied: 50mA Max. Measurement Room Temperature After Cooling For : Class I : 24 \pm 2 Hour Class II : 48 \pm 4 Hour s	
		Class II	X7R / X5R X6S / X5S	Within $\pm 12.5\%$					
			Y5V/Y5U/Z5U	Within $\pm 30 \sim 40\%$					
		Q Class I	C > 30 pF : Q ≥ 350 10 pF < C \leq 30 pF : Q $\geq 275 + 2.5 \times C$ C \leq 10 pF : Q $\geq 200 + 10 \times C$						
			Chip Array Capaitor C > 30 pF : Q ≥ 200 C \leq 30 pF : Q $\geq 200 + 10 / 3 \times C$						
Tan δ Class II	Temp. Char.	HI-V	50V	25V	16V	10V	6.3V		
	X7R/X5R X6S / X5S	2.5%	5%	7%	7%	10%	12.5%		
	Y5V	7.5%	7.5%	10.5%	12.5%	15%	20%		
	Y5U / Z5U	5%	6%	6%	6%	-	-		
Insulation Resistance	Minimum Insulation Resistance: 500M Ω or 25M $\Omega \times \mu\text{F}$ Product Whichever Is Smaller.								
15	Soldering Reference List	Size	Char. Temp	Capacitance			Condition		
				Reflow	Flow				
		0201	All	All			○	×	
		0402	All	All			○	×	
		0603	NP0 / X5R / X7R X6S / X5S	All			○	○	
				C < 1 μF	○	○			
			Y5V	C \geq 1 μF			○	×	
		0805	NP0 / X5R / X7R X6S / X5S	All			○	○	
				C < 4.7 μF	○	○			
			Y5V	C \geq 4.7 μF			○	×	
		1206	NP0 / X5R / X7R X6S / X5S	All			○	○	
				C < 10 μF	○	○			
			Y5V	C \geq 10 μF			○	×	
		1210 1808 1812 2220	All	All			○	×	

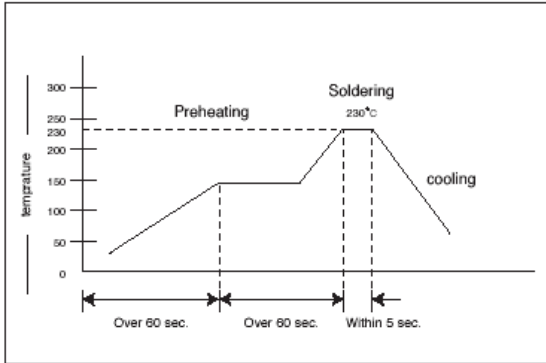


UWA Multi-Layer Ceramic Chip Capacitor

5-1 Soldering Recommendation

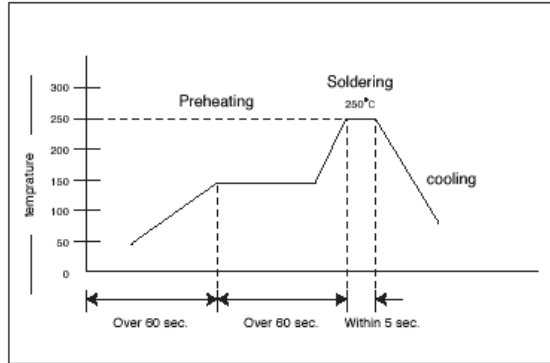
Sn/Pb Plating

Reflow



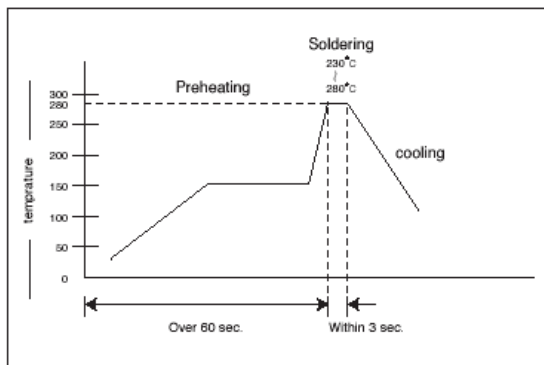
Pb-Free (Sn 100%) Plating

Reflow

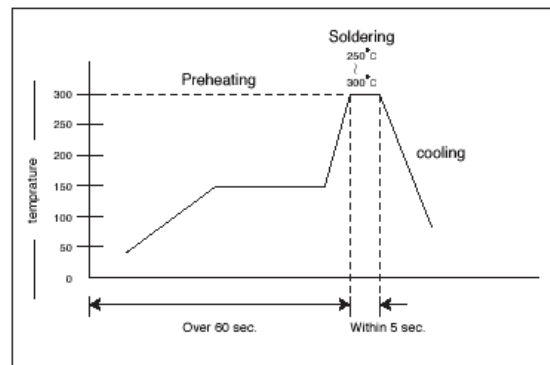


PS: It is suggest the number of Reflow time for all MLCC material : \geq 3 times

Solder Iron

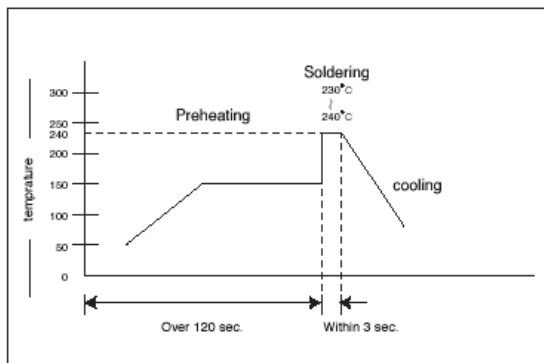


Solder Iron

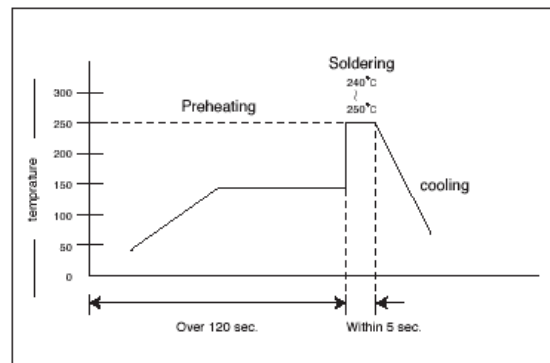


PS:If solder iron temperature about 380 °C , at first , to preheat MLCC within 1~3cm distance in radiant heat about 30~60 second , then to heat MLCC within 5seconds by solder iron (300~380 °C) .

Flow



Flow



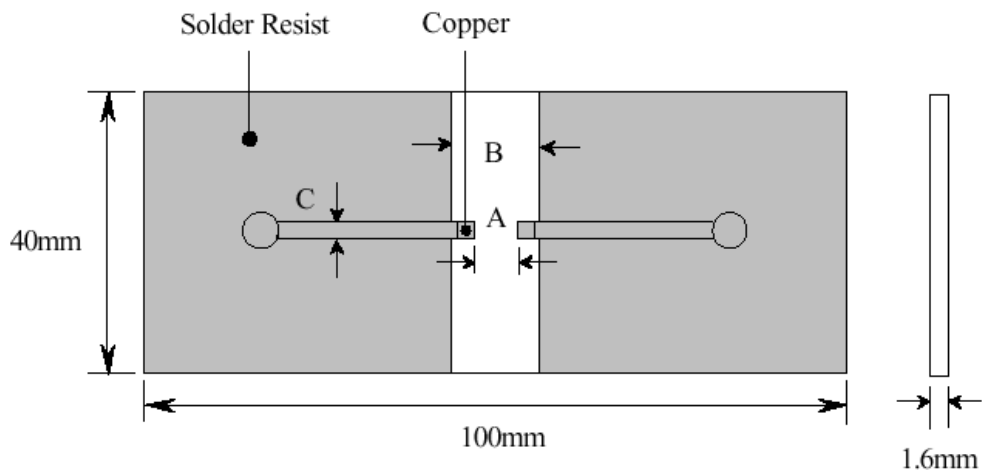


UWA Multi-Layer Ceramic Chip Capacitor

TABLE 1 Tan δ

X5R	
Rated voltage	Tan δ
DC \leq 10V	15.0%max
DC 16V	10.0%max
DC 25V	10.0%max
DC50V/35V	5.0%max
X7R/X6S	
DC \leq 10V	10.0%max
DC 16V	10.0%max
DC 25V	10.0%max
DC50V/35V	10.0%max
Y5V	
DC \leq 6.3V	20.0%max
DC 10V	20.0%max
DC 16V	12.5%max
DC25V	9.0%max
DC50V/35V	9.0%max

6. P.C. Board for Bending Strength Test



Unit: mm

Code	A	B	C
0201	0.2	1.0	0.3
0402	0.4	1.4	0.5
0603	1.0	3.0	1.0
0805	1.2	4.0	1.6
1206	2.2	5.0	2.0
1210	2.2	5.0	2.9
1808	3.5	7.0	2.5
1812	3.5	7.0	3.7
2220	4.5	8.0	5.6



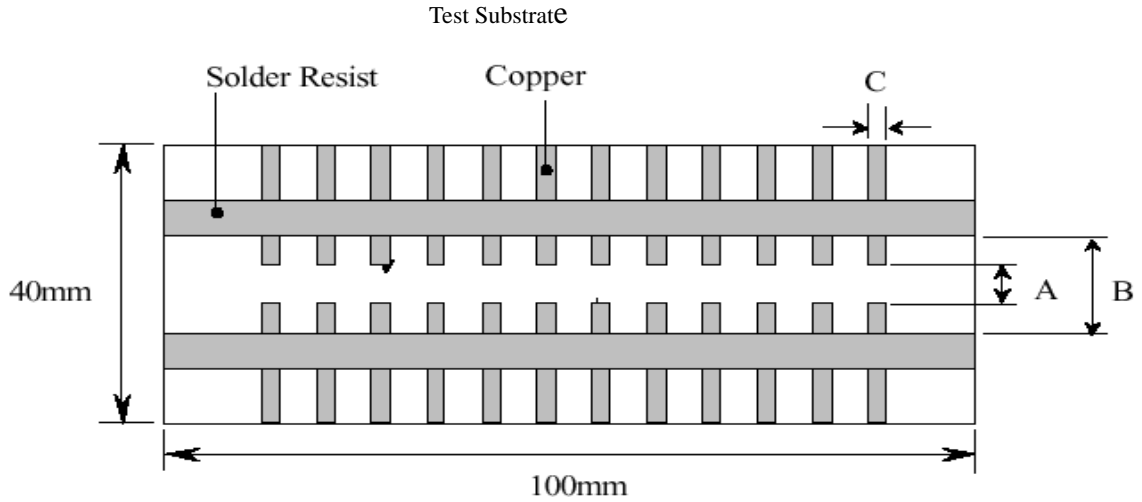
UWA Multi-Layer Ceramic Chip Capacitor

7. Test Substrate

Material: Glass Epoxy Substrate

■: Copper (Thickness: 0.035mm)

■: Solder Resist



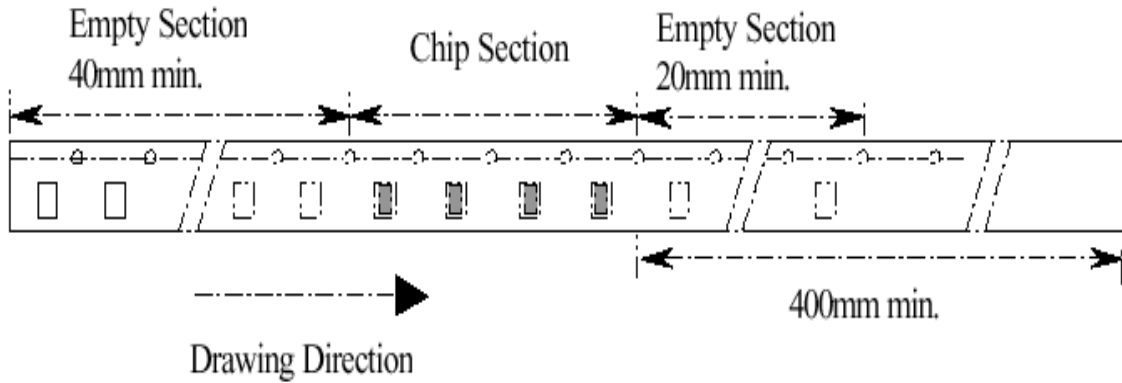
Unit: mm

Code	A	B	C
0201	0.2	1.0	0.3
0402	0.4	1.4	0.5
0603	1.0	3.0	1.0
0805	1.2	4.0	1.6
1206	2.2	5.0	2.0
1210	2.2	5.0	2.9
1808	3.5	7.0	2.5
1812	3.5	7.0	3.7
2220	4.5	8.0	5.6



UWA Multi-Layer Ceramic Chip Capacitor

8. Packaging



Material and Quantity

UNIT : PCS

Size	Thickness (mm)	7 # Reel		13 # Reel
		Paper Tape	Plastic Tape	Paper / Plastic
01005	$T \leq 0.22$	20K / Reel	-	100K / Reel
0201	$T \leq 0.33$	10K / 15K / Reel	-	-
0402	$T \leq 0.55$	10K / Reel	-	50K / Reel
0603	$T \leq 0.95$	4K / Reel	-	10K / 15K / Reel
0805	$T \leq 0.95$	4K / Reel	-	10K / 15K / Reel
	$0.95 < T \leq 1.45$	-	3K / 2K / Reel	-
1206	$T \leq 0.95$	4K / Reel	-	10K / Reel
	$0.95 < T \leq 1.45$	-	3K / 2K / Reel	-
	$T > 1.45$	-	2K / Reel	-
1210	$T \leq 1.45$	-	3K / Reel	10K / Reel
	$T > 1.45$	-	2K / Reel	4K / Reel
1808	$T \leq 1.45$	-	3K / Reel	10K / Reel
	$T > 1.45$	-	2K / Reel	4K / Reel
1812	$T \leq 2.22$	-	1K / Reel	4K / Reel
	$T > 2.22$	-	500 / Reel	4K / Reel
2220	$T \leq 2.22$	-	1K / Reel	2K / Reel
	$T > 2.22$	-	500 / Reel	2K / Reel

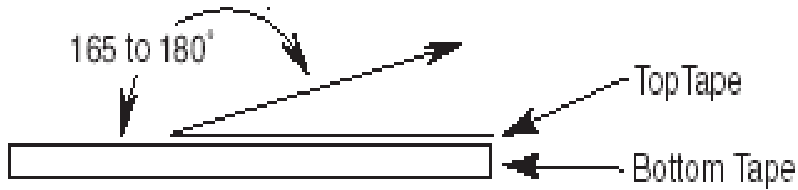


UWA Multi-Layer Ceramic Chip Capacitor

8-1. Cover Tape Reel Off Force

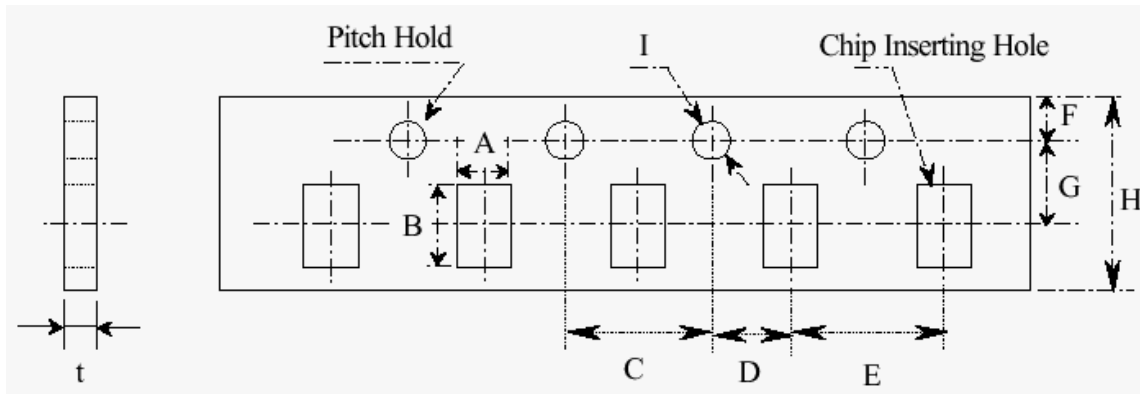
Peel-Off Force : $5 \text{ g} \cdot f \leq \text{Peel-Off Force} \leq 70 \text{ g} \cdot f$

Cover Tape reel Off Force



The for peel off cover tape is 5 to 70 grams in the arrow direction.

8-2. Paper Tape



Unit: mm

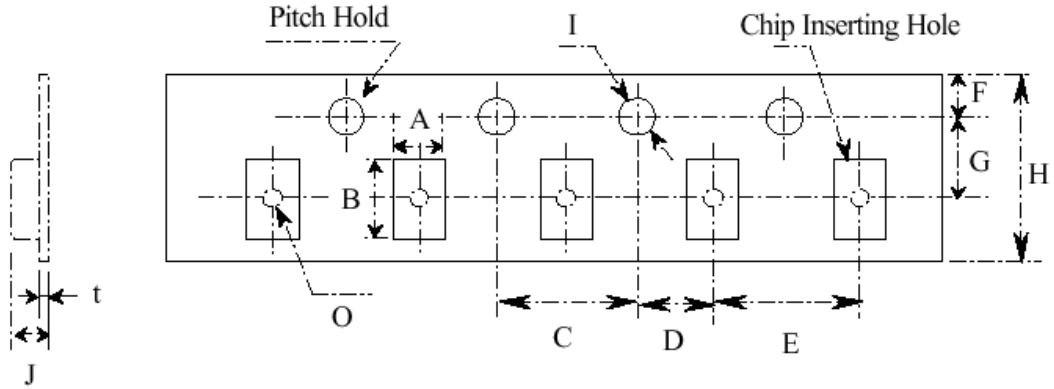
Code	A	B	C	D	E
01005	0.25±0.02	0.45±0.02	4.0±0.1	2.0±0.1	2.0±0.1
0201	0.37±0.03	0.67±0.03			
0402	0.61±0.10	1.2±0.1			
0603	1.10±0.20	1.9±0.2			4.0±0.1
0805	1.50±0.20	2.3±0.2			
1206	1.90±0.20	3.5±0.2			
1210	2.90±0.20	3.6±0.2			

Code	F	G	H	I	t
0201	1.75±0.1	3.5±0.05	8.0±0.3	φ1.5+0.1/-0	1.1max
0402					
0603					
0805					
1206					
1210					



UWA Multi-Layer Ceramic Chip Capacitor

8-3. Plastic Tape



Unit: mm

Code	A	B	C	D	E	F
0805	1.5±0.2	2.3±0.2	4.0±0.1	2.0±0.05	4.0±0.1	1.75±0.1
1206	1.9±0.2	3.5±0.2				
1210	2.9±0.2	3.6±0.2				
1808	2.5±0.2	4.9±0.2			8.0±0.1	
1812	3.6±0.2	4.9±0.2				
2220	5.4±0.2	6.1±0.2				

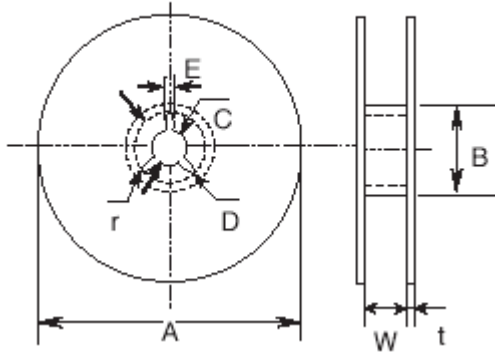
Code	G	H	I	J	t	O
0805	3.5±0.05	8.0±0.3	$\phi 1.5 + 0.1 / - 0$	3.0 max.	0.3 max.	0.15 min.
1206						
1210						
1808	4.0 max.					
1812						
2220						
		5.5±0.05	12.0 + 3 / - 0			



UWA Multi-Layer Ceramic Chip Capacitor

8-4. Reel Dimensions

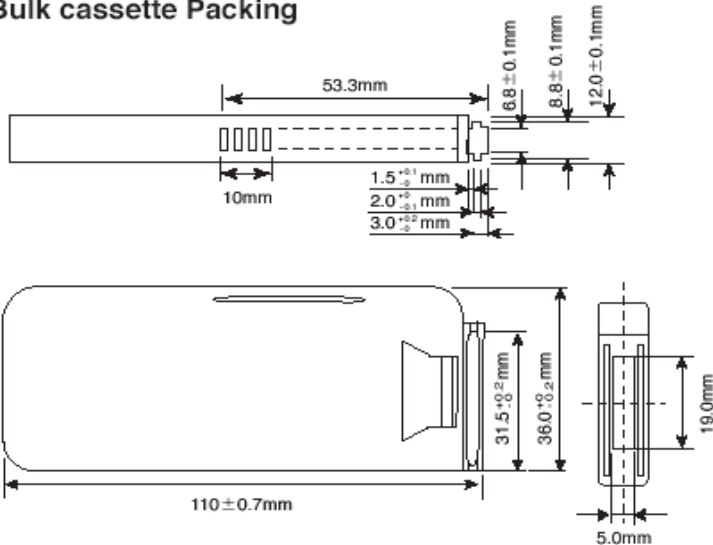
Material: Paper, Plastic



Tape Size	7 // Reel		13 // Reel	
	8mm	12mm	8mm	12mm
A	178±2		330±2	
B	50±2		60±2	
C	13±0.5		13±0.5	
D	21±1		21±1	
E	2±0.5		2±0.5	
W	10±1.5	14±2	10±1.5	14±2
T	1.5±0.5		2±1	
r	1.0		1.0	

8-5. Bulk Cassette Quantity

Bulk cassette Packing



Type	Thickness (mm)	Pcs / Case
0402	0.5	50K
0603	0.8	15K
0805	0.6	10K
	0.85	10K
	1.25	5K

9. Precaution of Usage

9-1. Storage

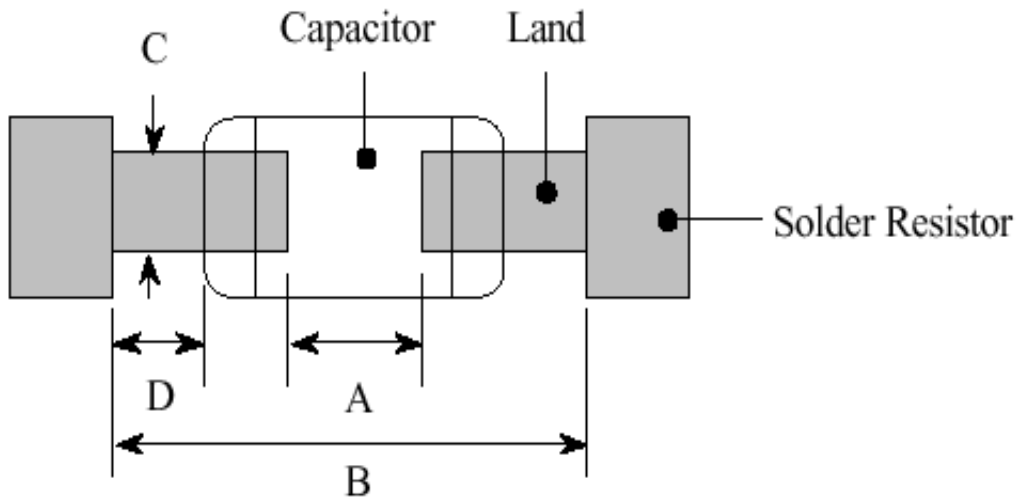
Store the capacitors where the temperature and relative humidity don't exceed 40°C and 70%RH. We recommend you use capacitors within 6 months from the manufactured date. In case of packaging, don't the last wrapped, Polyethylene bag, till just before using. If it is opened, seal it as soon as possible or keep it in a desiccant with a desiccation agent.



UWA Multi-Layer Ceramic Chip Capacitor

9-2. Size and recommend land dimensions.

Code	Chip Capacitor		Land			
	L	W	A	B	C	D
0201	0.60	0.30	0.2~0.3	0.9~1.1	0.2~0.3	0.1~0.3
0402	1.00	0.65	0.3~0.5	1.3~1.5	0.3~0.5	0.1~0.3
0603	1.60	0.80	0.6~0.8	1.9~2.1	0.6~0.8	0.2~0.5
0805	2.00	1.25	0.8~1.2	2.4~3.2	0.9~1.2	0.2~0.6
1206	3.20	1.60	1.8~2.5	3.8~4.8	1.2~1.6	0.3~0.8
1210	3.20	2.5	1.9~2.6	3.9~4.9	1.9~2.5	0.3~0.8
1808	4.50	2.00	2.4~3.4	5.4~6.0	1.7~2.0	0.5~1.3
1812	4.50	3.20	2.5~3.5	5.5~6.1	2.3~3.2	0.5~1.3
2220	5.70	5.00	2.7~4.2	6.7~8.3	3.5~5.0	0.5~1.3

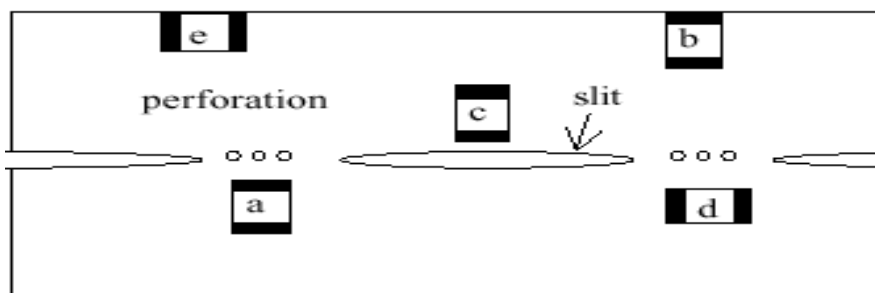


Unit: mm

9-3. Mechanical strength varies according to location of chip capacitors the P.C. board.

Design layout of components on the PC board to minimize the stress imposed on the wrap or flexure of the board
 Component layout close to board break

Susceptibility to stress is in the order of: a>b>c≠d>e





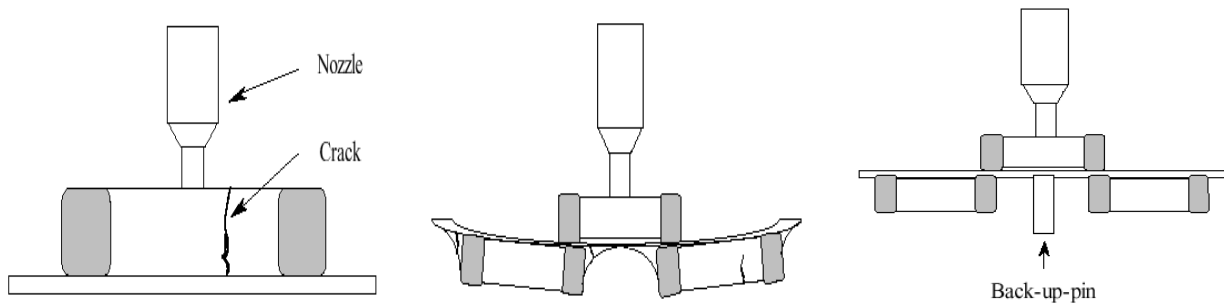
UWA Multi-Layer Ceramic Chip Capacitor

9-4. Layout Recommendation

Example	Use of Common Solder Land	Solder With Chassis	Use of Common Solder Land With Other SMD
Need to Avoid			
Recommendation			

9-5. Mounting

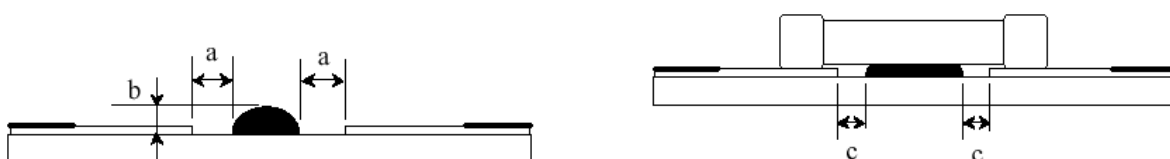
Crack is caused by impact load due to suction nozzle at the mounted. In mounting an element to board, if the low dead point is too low, excessive stress is applied to element. This will cause cracking. In this case, it is required to shift the low dead point of a suction nozzle to the upper surface of board so that warping of board is eliminated. Nozzle pressure is adjusted to 1N to 3N (static load) during mounting.



To Fix Board with Support Pin (OK)

If board is warped during mounting, crack or peeling of soldering will be caused. To avoid this, it is required to fix the board with back up pins or the like to avoid warping. Also, similar precautions are required when inserting a part with lead.

9-6. Amount of Adhesive



Example : 0805 & 1206 Size MLCC	
A	0.2mm (min)
B	70 ~ 100 uM
C	Do Not Touch The Solder Land



UWA Multi-Layer Ceramic Chip Capacitor

9-7.Soldering

9-7-1.Avoiding Thermal Shock

(a) preheat Condition

Carefully perform pre-heating so that the temperature difference (ΔT)between the solder and component surface should be in the follow range.

Soldering Method	3.2x1.6mm max.	3.2x1.6mm min.
Reflow method	$\Delta T \leq 190^{\circ}\text{C}$	$\Delta T \leq 190^{\circ}\text{C}$
Immersion method	$\Delta T \leq 150^{\circ}\text{C}$	$\Delta T \leq 100^{\circ}\text{C}$

(b) Cooling Condition

Natural cooling using air is recommended. If the chips arid dipped into a solvent for cleaning, the temperature difference (ΔT)must be less than 100°C

9-7-2. Recommend Soldering Profile By various Methods

Infrared reflow soldering standard condition Iron/immersion soldering standard condition

9-7-3. Amount of Solder

Excessive solder will induce higher tensile force in chip capacitor when temperature change and it may result in chip cracking. In Sufficient solder may detach the capacitor from the P.C. board.

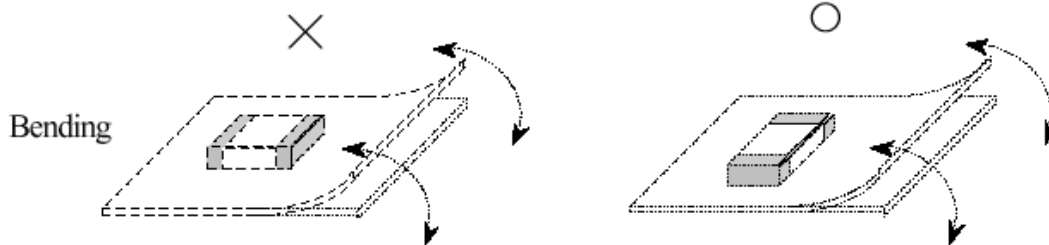
PS: It is suggest the number of Reflow time for all MLCC material : ≤ 3 times .

PS: If solder iron temperature about 380°C , at first , to preheat MLCC within 1~3cm distance in radiant heat about 30~60 second, then to heat MLCC within 5seconds by solder iron ($300\sim 380^{\circ}\text{C}$) .

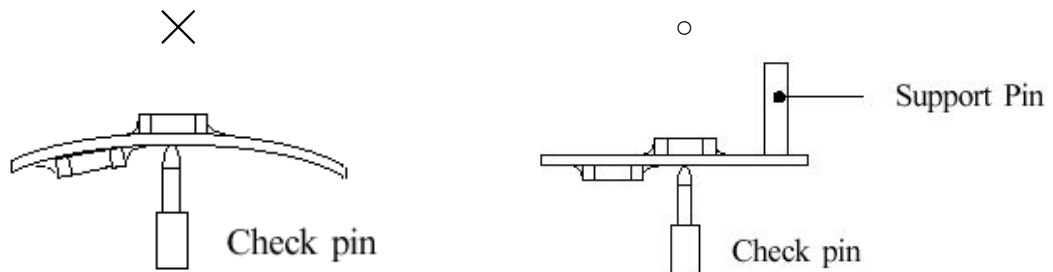
Excessive Solder	
Adequate	
Insufficient Solder	
Solder buildup by Reflow method	

10. Caution: Handling after chip mounted

10-1. Please pay attention put the component lateral to the direction in which stress acts.

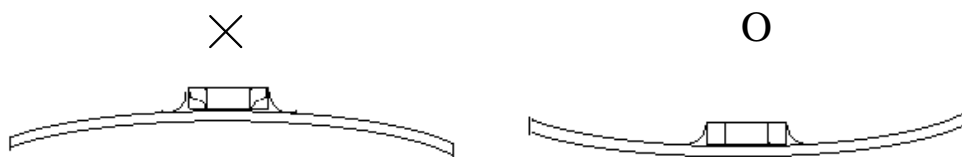


10-2. Crack will be caused if board is warped due to excessive load by check pin.



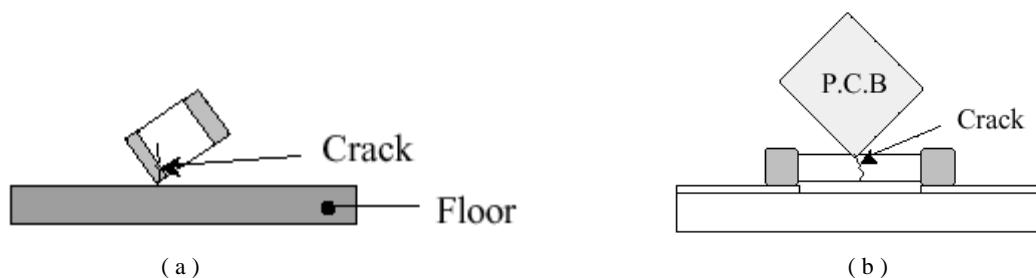
10-3. Mechanical stress due to warping and torsion by dividing.

- (a) Crack occurrence ratio will be increased by manual separation.
- (b) Crack occurrence ratio will be increased by tensile force, rather than compressive force.



10-4. Handling to Loose Chip Capacitor

- (a) IF dropped the chip capacitor may crack.
- (b) Piling the P.C. board after mounting for storage or handling, the corner of the P.C. board may hit the chip capacitor of another of board to cause crack.





UWA Multi-Layer Ceramic Chip Capacitor

Lipers Enterprise Co., Ltd.

HQ: 2F., No.2, Aly. 1, Siwei Ln., Zhongzheng Rd., Xindian Dist., New Taipei City R.O.C.

TEL: +886-2-2218-9555 FAX: +886-2-2219-5666 www.lipers.com.tw